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**Topic: Logic Circuit Implemetation**

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**Sub Code: 19CS211 Sub Title: COA**

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With respect to a smart home imitative, we have to design an automatic water level controller with the following requirements. Overhead tank has level sensors at two different positions labeled LLS (Low Level Sensor) and HLS (High Level Sensor). Whenever the water falls below LLS, Motor should be switch on (MOut) and whenever the water raises above HLS, Motor (MOut) should be switched off. Whenever the water level remains between LLS and HLS, the status of the motor should remain in its previous state (PS) (No change in the state of the MOut). Three inputs PS, LLS, HLS and one output MOut. Derive the digital logic circuit for the above scenario, implement and test your digital design with the help of iVerilog.

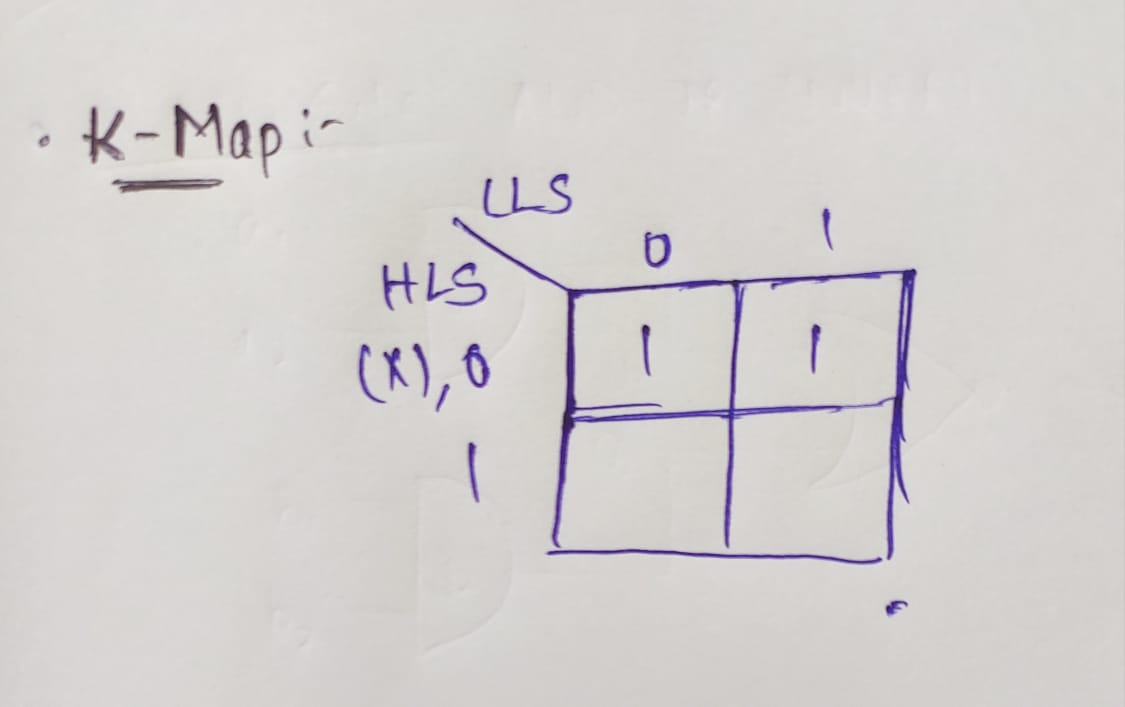
**TRUTH TABLE:**

|  |  |  |  |
| --- | --- | --- | --- |
| PS | LLS | HLS | MOut |
| X | 0 | X | 1 |
| 0 | 1 | 0 | 0 |
| 1 | 1 | 0 | 1 |
| X | 1 | 1 | 0 |

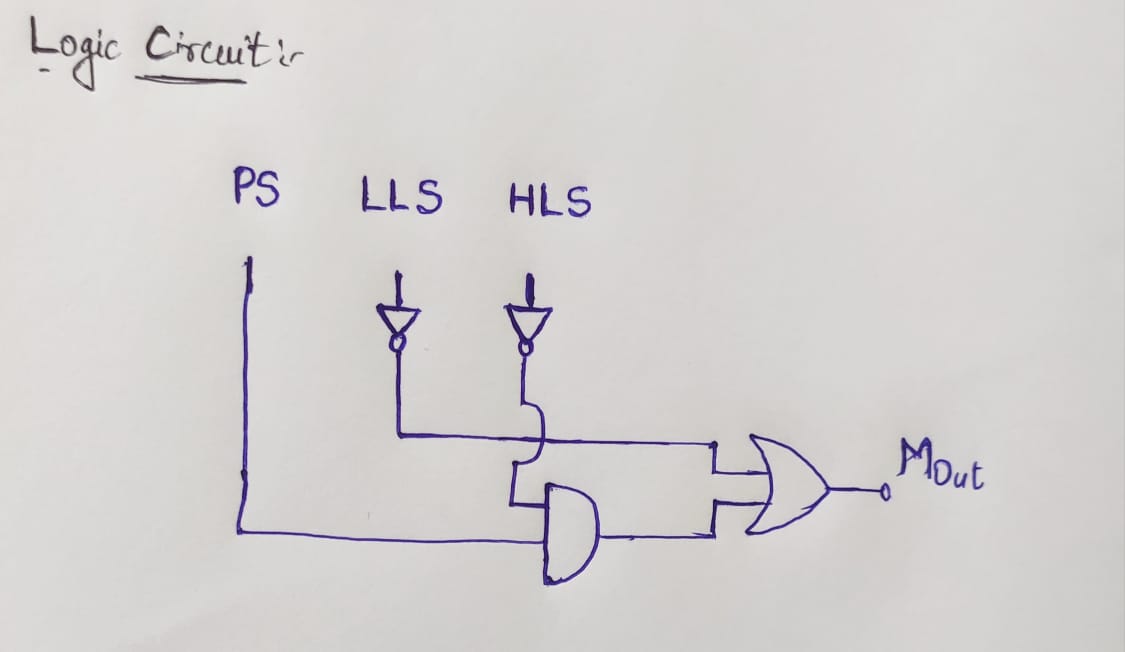
**Logic equation:**

**MOut =** + (PS & )

**K-Map:**



**Logic circuit:**



**iVerilog Code:**

module watercontroller(Mout, PS, LLS, HLS);

input PS, LLS, HLS;

output Mout;

assign Mout = !LLS + (PS & !HLS);

endmodule

**TestBench :**

**Test bench:**

module eval1\_tb;

wire t\_Mout;

reg t\_PS, t\_LLS, t\_HLS;

watercontroller eval1\_tb(.PS(t\_PS), .LLS(t\_LLS), .HLS(t\_HLS), .Mout(t\_Mout));

initial

begin

$monitor(t\_PS, t\_LLS, t\_HLS, t\_Mout);

t\_PS = 1'b0;

t\_LLS = 1'b0;

t\_HLS = 1'bX;

#5

t\_PS = 1'b0;

t\_LLS = 1'b1;

t\_HLS = 1'b0;

#5

t\_PS = 1'b1;

t\_LLS = 1'b1;

t\_HLS = 1'b0;

#5

t\_PS = 1'bX;

t\_LLS = 1'b1;

t\_HLS = 1'b1;

end

endmodule

**Output:**

